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STATIC

DC TO SINUSOIDAL AC

CONVERSION

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OTS PRICE

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MICROFILM $ .80

The need to reduce size and weight of electrical equipment is probably most felt when such equipment is intended for use aboard a space vehicle. Electrical Engineers are continuously challenged to invent means whereby such equipment can be made very light and compact without incurring any adverse losses in other important qualities such as efficiency, reliability, and simplicity.

In anticipation of the need for high-power AC supplies, the problem of conversion from available direct voltage to alternating voltage having a specified frequency has, in this sense, been of particular interest to the writer. This problem was pursued closely only for the duration of the summer of 1962. Consequently, the findings which will be summarized in this section of the progress report are quite preliminary in nature and much work need still be done before satisfying results will be realized.

REDUCTION OF SIZE AND WEIGHT

The Filter. In a magnetically coupled static d-c to a-c inverter, the magnetic core with its windings and the output filter constitute the major portion of the bulk of the converter. Hence, especially in high-power systems, any reasonable percentage weight reduction in these two items may very well prove to be of considerable value. Thus the inverter transformer core and the filter receive first attention.

Let the required output voltage be a sinusoid of frequency f as shown in Figure 1. Superimposed on the sine wave shown in Figure 1 is a square wave which is often the shape of the unfiltered output of a static inverter. The harmonic content of such a wave is 48.4%(1) of which the third harmonic constitutes a large portion. With a semi-square wave output as depicted in Figure 2, the third harmonic is eliminated and the harmonic content is reduced to 30.9%.(1) Further reduction of harmonics may be achieved if the output of the inverter is made to be a stepped wave such as shown, for example, in Figure 3(a) or 3(b) where, by proper adjustment of the step heights, it is possible to eliminate all odd harmonics below the 11th and reduce the harmonic content to 15.1%.(1),(2),(3) In high-power circuits this means a considerable reduction in the size and weight of the filter required to yield a total harmonic distortion representative of aero-space specifications.(1)

The Magnetic Core and Winding: It is known that for a certain input voltage, the size of a saturable core in an inverter is directly proportional to the time (subsequently represented by t_c) needed for the core to be reset from the maximum negative flux-excursion level ($-\phi_m$) to the maximum positive flux-excursion level ($+\phi_m$), (or vice versa). This time t_c is in turn directly proportional to the number of turns on the input winding of the inverter. Thus, the size and weight of the core and winding may be reduced by shortening the time t_c.

STEPPED-WAVE SYNTHESIS

Conventional Method:

Stepped waves of the form illustrated in Figure 3 are usually synthesized by summing a number of square waves that are properly displaced from one another in time.[(1),(2)] To clarify, Figure 4 shows how five square waves, displaced progressively by 36 degrees are summed to yield a stepped wave having five steps per half cycle. In an inverter system each of these square waves would represent the output voltage of one inverter stage. Thus, the outputs are summed in series to yield the stepped-wave approximation of the required sinusoid.

It should be noted that according to this scheme of synthesis all the constituent square waves have the same frequency f, namely that of the required sinusoid. Since there is no dwell time in any of these constituent square waves, the flux in the core of each inverter stage must change by $2\phi_m$ in 1/2f seconds regardless of how many steps the resultant stepped wave is made. This immediately places a restriction on the core size of every inverter in the system. The minimum size and weight of the magnetic cores and the windings in the inverter system are then limited by the specification on the frequency of the sinusoidal output. In contrast, the number of steps is not limited by the output frequency and, at least in principle, this number can be made as large as one pleases, i.e. the stepped wave can be made so close an approximation to a sinusoid that no filter is necessary for all practical purposes. What limits the number of steps, as far as size and weight are concerned, is the fact that a point is reached where the increment in the size and weight of the overall system due to the addition of one more inverter stage, (corresponding to one more step,) is more than the corresponding decrement in the size and weight of the output filter.

Proposed Method:

To achieve a reduction in the size and weight of the magnetic cores and windings in addition to that of the filter each inverter stage must operate such that a change of $2\phi_m$ in the core flux take place in a period of time t_c that is considerably shorter than 1/2f where f is the frequency of the desired sinusoidal output. A method is proposed whereby the time t_c is made equal to 1/2nf where n is the number of steps per half cycle of the synthesized stepped wave. By this method the stepped wave is synthesized as illustrated in Figure 5 for the case of six steps. It is worthy of notice that the number of stages is one less than the number of steps.

A two-stage inverter is adequate for experimentally illustrating this method of synthesis. The output of such an inverter would be a 3-step wave as shown in Figure 6(a). The problem is then twofold: first, to devise means whereby the inverter switching elements (in this case SCR's) may be triggered properly, both sequence-wise and time-wise, so that each stage yields the desired output; second, to devise means whereby the individual outputs can be summed and successfully applied to a load.

This problem received first attention and circuitry was devised to accomplish, at least in principle, the required task. A two-stage inverter is shown in block-diagram form in Figure 7. The stages operate indentically and hence the operation during one complete cycle will be described for one stage only.

OPERATION OF ONE INVERTER STAGE

Basic components in one inverter stage are:[4] Two-core saturable transformer and windings, 2 silicon-controlled rectifiers, and two turn-off capacitors. The circuit configuration is shown in Figure 8, and the operation during one cycle is described briefly in the following. (For more details the reader is referred to Ref. 4).

Let stage #1 be considered. Initially both SCR's are in the blocking state, each of the capacitors C1A and C1B is charged to E volts, and the cores are saturated to the left. Referring to Figure 6(b), at t_1 a pulse of very short duration, short compared to t_c, arrives at the gate of SCR1A. As soon as this SCR starts conducting capacitor C1A is discharged through N4' until its voltage becomes equal to the forward voltage drop across the SCR, and the small core T2' is momentarily reset to the right. But while SCR1A is conducting voltage is induced in the output winding N3', part of which is applied to the reset winding N6' in such a way as to reset core T2' to the left. After a period of time t_c core T1' saturates to the right, whence the flux change must take place in core T2' to support the input voltage. This causes an induced voltage to appear on winding N4' with such a polarity as to back-bias SCR1A. This results in a backward flow of current through the SCR which thereby is turned off. (It will be shown later how the back-bias voltage that is made to appear across SCR1A during turn off can be adequately used to turn on an SCR in another stage.)

Again referring to Figure 6, the second half cycle of operation for the first stage starts with triggering SCR1B at t_2. The events during the second half cycle are similar to those during the first with C1B and SCR1B replacing C1A and

SCR1A respectively. The output of the first stage is represented by pulses 1A and 1B.

TRIGGERING ONE SCR FROM ANOTHER

A back-bias voltage applied to an SCR for a very short duration in order to turn it off may be successfully used to turn on another SCR since, in general, the turn-on time for an SCR is shorter than the turn-off time. A simple arrangement to accomplish this is shown in Figure 9. Here, the voltage V is conveniently chosen such that it tend to forward bias the gate of SCR2A during the interval of time when it is desired that this SCR begin to conduct and that it tend to back-bias the gate otherwise. Under this condition, when SCR1A is being turned off and its anode becomes negative with respect to ground, base current flows in the base circuit of transistor Q1. This transistor then conducts the gate current for SCR2A and the SCR turns on. As long as SCR1A is conducting in the forward direction, Q1 is back-biased and no gate current can flow in the gate of SCR2A.

DIRECTING THE FIRST TRIGGER-PULSE

In describing the operation of one inverter stage (Fig.8) it was mentioned that initially the cores are saturated in a predetermined direction and hence a certain SCR had to be triggered first. As will be shown later the triggering scheme for the proposed inverter configuration is such that pulses of short duration, to be derived from a Royer circuit square-wave voltage output with a constant frequency equal to the desired sinusoidal output frequency, are sequentially directed to two SCR's, one in each inverter stage. Thus, without specific reference to location of SCR's, it will be shown how one of two SCR's is always triggered first, regardless of the initial polarity of the square-wave voltage from which the trigger pulses are derived.

This is done very simply by the circuit shown in Figure 10. Here, capacitor C3 is initially discharged by virtue of the presence of the bleeder resistor R9. If, at the beginning of operation, the dotted ends of the output windings N7 and N8 of the Royer circuit are made positive with respect to the other ends then a pulse of current flows through N7 via the series combination C3, gate of SCR1, D4, R8, and D5. The time constant of R8 and C3 is very small so that the current pulse is of very short duration and C3 charges quickly to approximately V volts with its bottom plate positive. As long as the dotted end of N8 is positive, Q3 is reverse biased and hence the capacitor cannot discharge through it. But when the polarity of the voltages on N7 and N8 reverses during the next half cycle Q3 becomes properly biased for conduction and C3 thus discharges through the series combination Q3, R8, gate of SCR2, and D3. If at the beginning of operation, on the other hand, the dotted ends of N7 and N8 are made negative none of the gates receives a current pulse since D5 blocks the voltage on N7 and there is no charge on C3 to be discharged through the properly biased Q3.

TO SUM THE OUTPUTS

Two consecutive output pulses, one from each inverter stage, occur during every half cycle of operation as indicated in Figure 6. An output pulse from an inverter stage coincides with the conduction of one of its SCR's. At the end of each output pulse both cores in the inverter stage are left saturated in one direction where as explained in the operation of one inverter stage, they must remain until the second half cycle. Since the output windings must be connected in series in order to get the desired stepped-wave output, it will be shown in the following that this raises the problem that the output voltage pulse from one stage tends to reset the cores in the other during an undesirable interval of time in the half cycle. For proper operation it is therefore necessary to bypass the output windings of the inverter during such critical time intervals. To illustrate with a diagram why and how this is done reference is made to Figure 11. For simplicity both cores of each inverter stage are represented in this diagram by one.

Because of symmetry, the operation of the output circuit shown in Figure 11 will be described only for one half cycle. The cores are initially saturated to the left. The first output voltage pulse appears on output winding N3' and tends to make current flow into the dotted terminal of this winding. For this current the core in stage #2 is saturated and hence presents a very low impedance path. Clearly neither SCR1C nor SCR2C can conduct this current. Thus, the path of current is through N3',N3" and the load. The first voltage ends with the core of stage #1 saturated to the right. An output voltage pulse then appears on output winding N3" and tends to make current flow into the dotted terminal of this winding. If this current is allowed to flow through N3' the core of stage #1 will be reset which is not desired. Therefore, part of the voltage on N3' is used to trigger the gate of SCR2C which then bypasses the current around N3' and the core of stage #1 can be reset only very slightly due to the forward voltage drop across SCR2C. Clearly SCR1C cannot conduct if its gate signal during this time is made extremely small. At the end of this second output voltage pulse the core of stage #2 is left saturated to the right.

Thus, during the first half cycle the cores in both inverter stages are saturated to the right and remain so until output voltage pulses with reverse polarity appear during the second half cycle. The operation during the second half cycle is similar to that during the first with the current direction reversing and SCR1C assuming the role of bypassing the current around N3".

THE OVERALL TWO-STAGE INVERTER

Figure 12 shows the complete circuit of the two-stage inverter. The only components here that have not been discussed previously are R7 and windings N9 and N10 in the trigger circuit. The resistance R7 is of such a value as to allow magnetizing currents to flow through windings N2' and N2" when switch S is closed momentarily. Thus brief closure of switch S before starting the trigger circuit guarantees the resetting of both inverter cores to the proper direction.

Circuit operation is started when, after energizing the (Royer) trigger circuit, the dotted end of N7 becomes positive with respect to the undotted end. Inspection of polarity markings on N9 and N10 then shows that the voltages on these windings have the qualities stated in the section on "Triggering One SCR From Another".

Filtering The Stepped Wave Output

Time did not allow any work on this problem.

TESTS AND FINDINGS

The circuit shown in Figure 12 was built and tested very briefly, without a filter, with both purely resistive loads and slightly inductive loads. Operation was stable for medium loads only. Time limitations did not allow a deep and thorough investigation of circuit irregular behavior with large loads.

CONCLUSIONS

Much work need still be done before any valid conclusions can be drawn. It is strongly believed, however, that further investigation into this problem may lead to the introduction of few modifications into the circuit which will make it operate reliably and efficiently.

Work in this area was terminated in September, 1962.

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(1) Static Inverter With Neutralization of Harmonics, Andress Kernick, J. L. Roff, T. M. Heinrich. AIEE TRANSACTIONS, (Applications and Industry), May 1962, pp. 59-68.

(2) Static Power Inverter Utilizing Digital Techniques and Harmonic Cancellation, D. L. Anderson, A. E. Willis, C. E. Winkler. AIEE Conference Paper No. CP 62-1148.

(3) Method of Optimizing the Waveform of Stepped-Wave Static Inverters, P. D. Corey, AIEE Conference Paper No. CP 62-1147.

(4) A Self-Oscillating Inverter Using a Saturable Two-Core Transformer To Turn Off Silicon Controlled Rectifiers, E. T. Moore, T. G. Wilson, R. W. Sterling. AIEE Transactions Paper No. 62-1029.

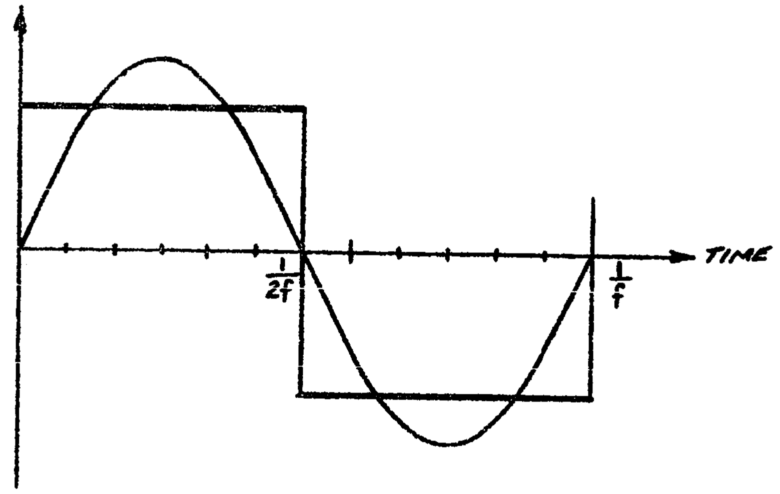


Fig. 1 A sine wave and a square wave.

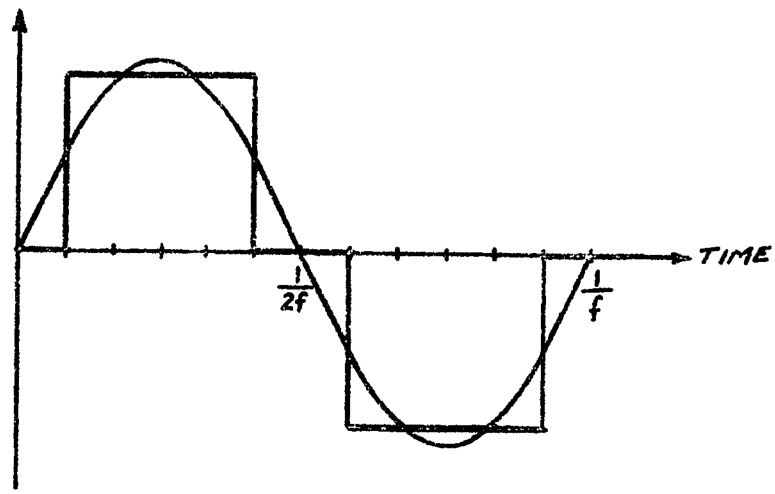


Fig. 2 A sine wave and a semi-square wave.

(a)

(b)

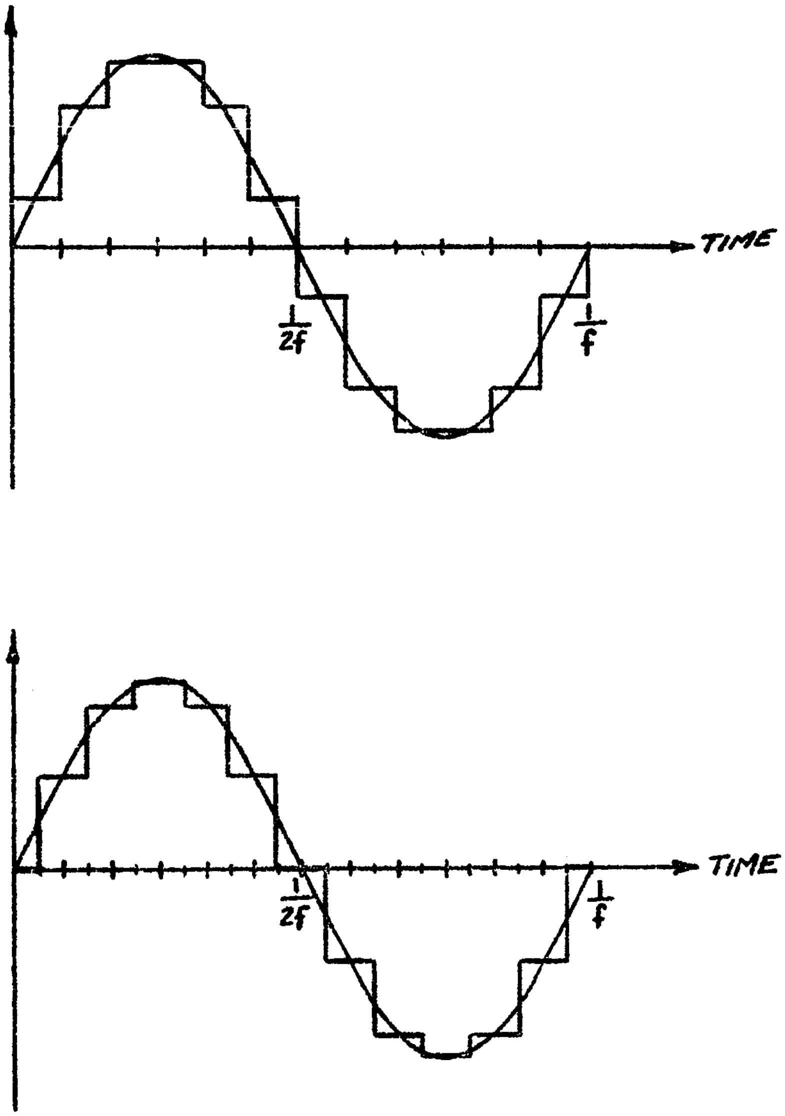


Fig. 3 (a) A Stepped Wave and A Sine Wave

(b) Alternative Steps

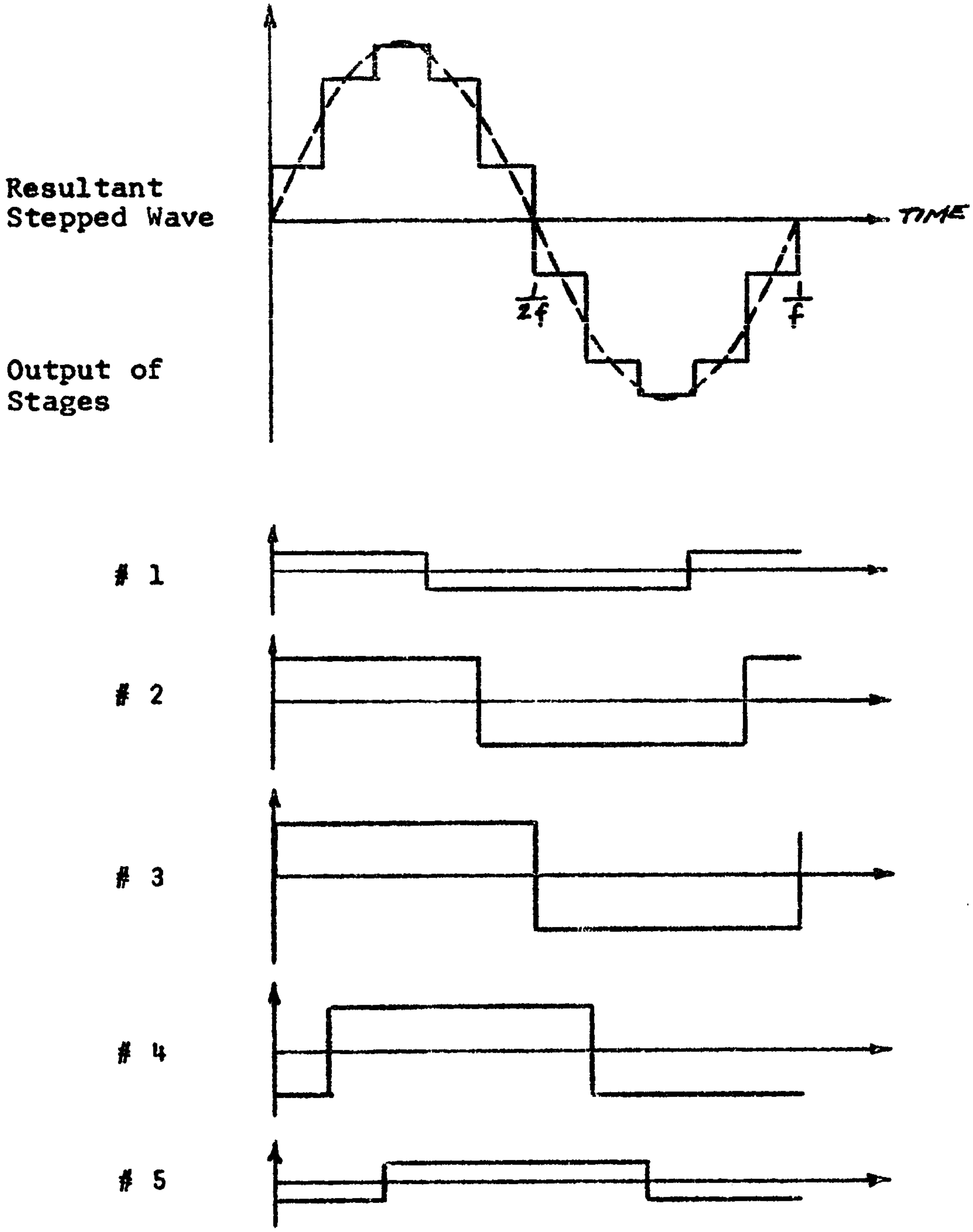


Fig. 4 A five-step stepped wave and constituent square waves.

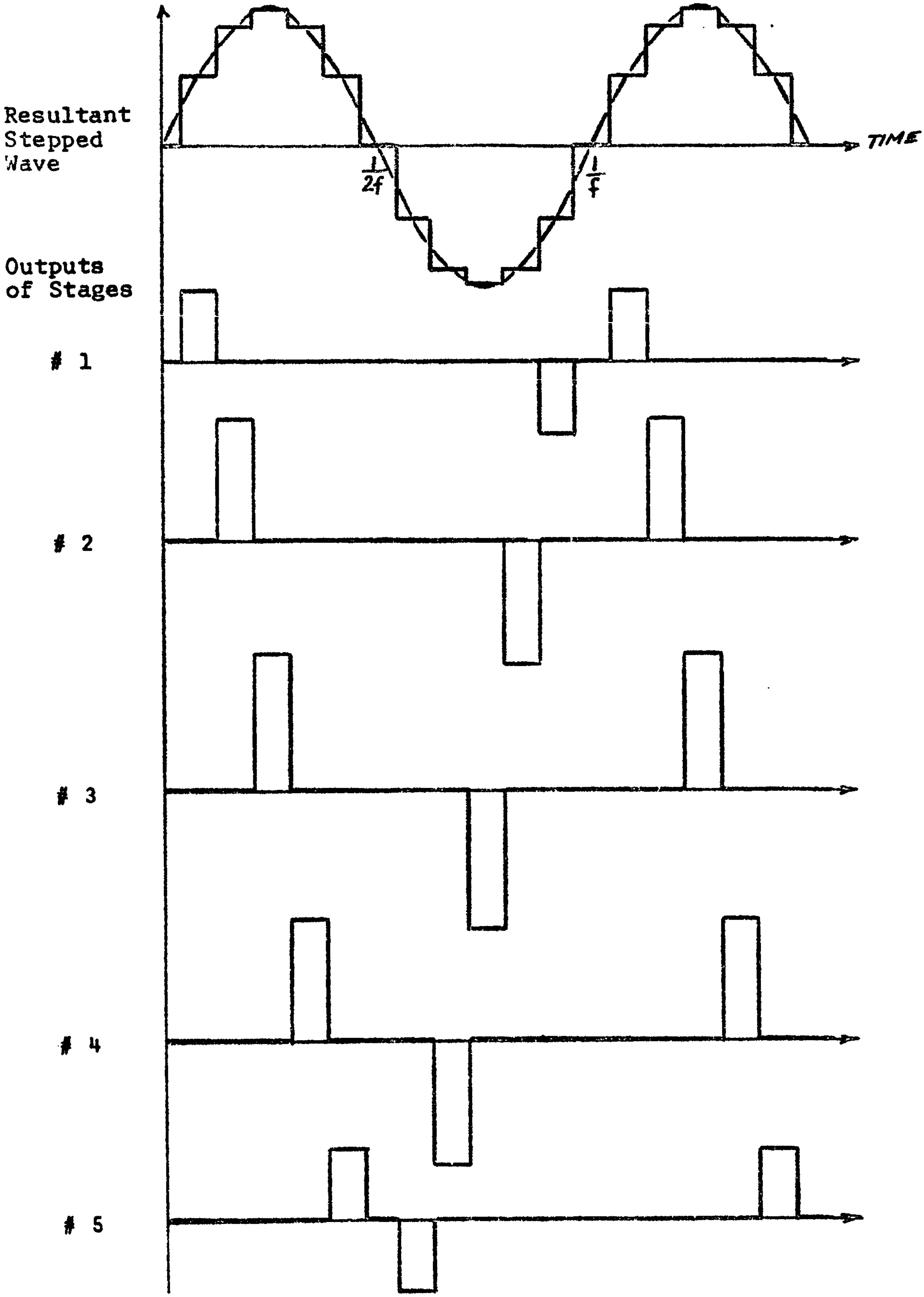


Fig. 5 Another method of synthesis of a stepped wave.

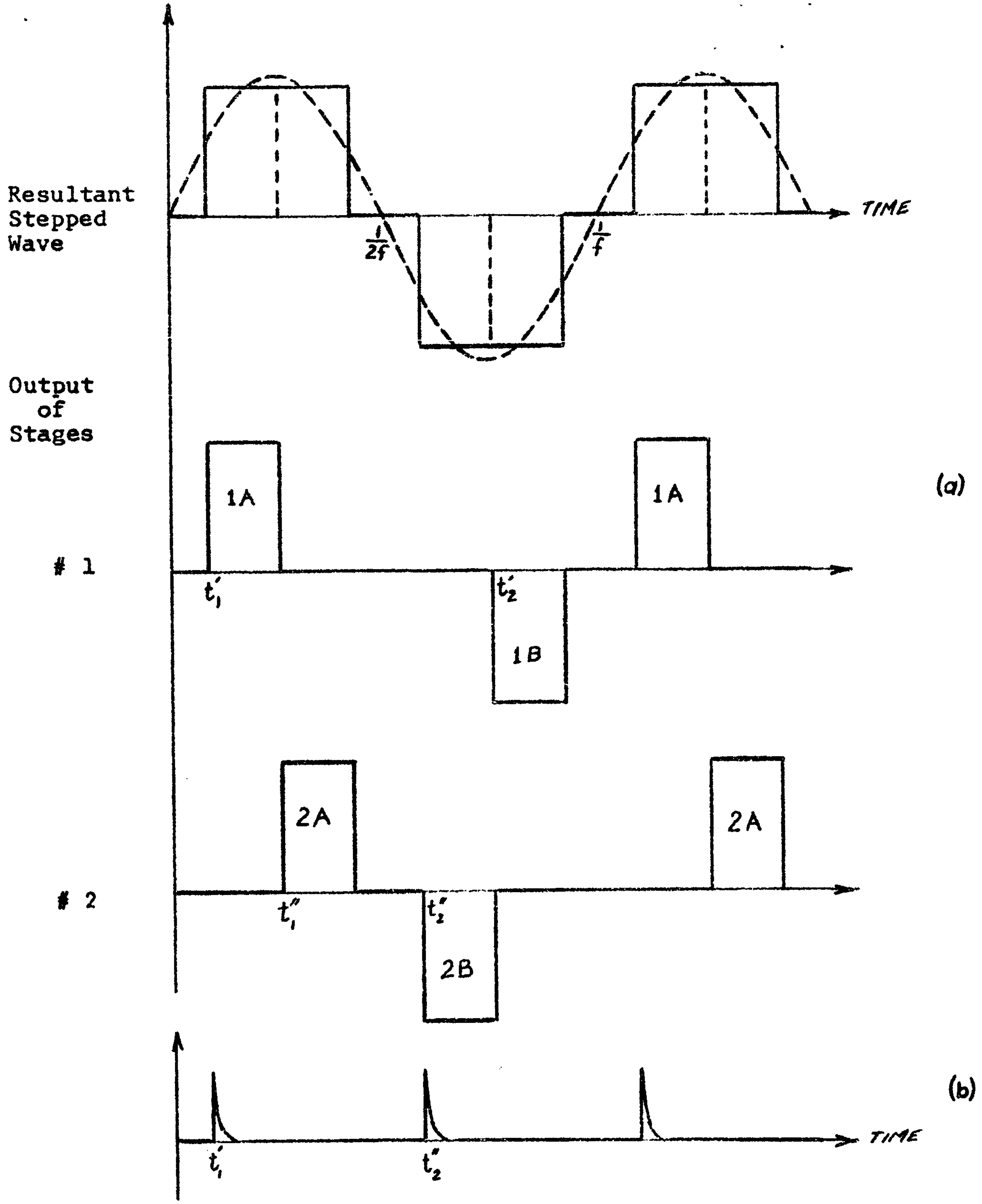


Fig. 6 (a) A 3-step stepped wave and constituents

(b) Trigger pulses.

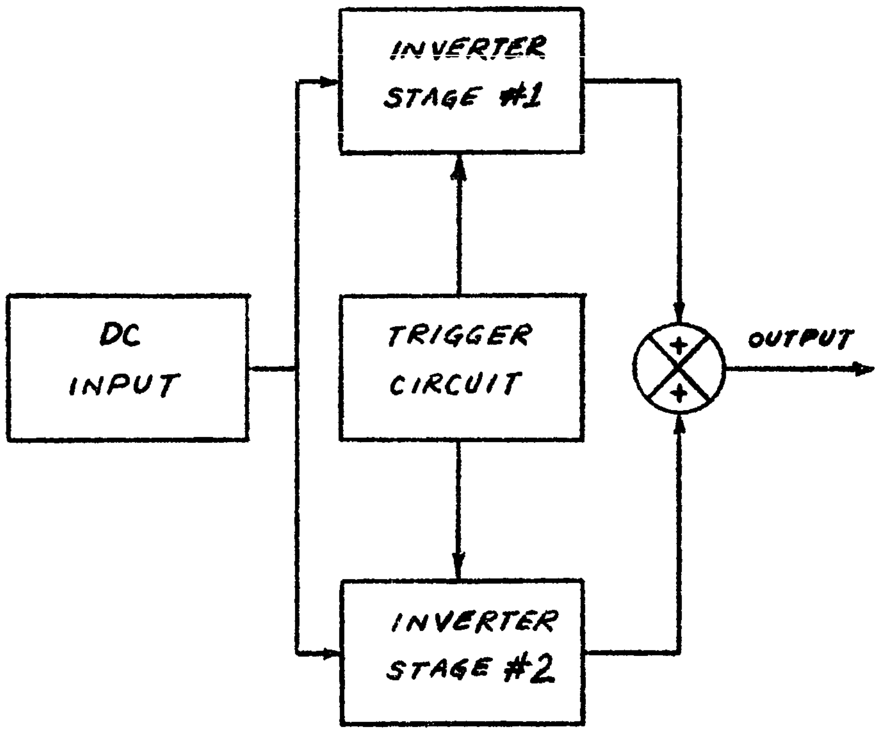


Fig. 7 Block Diagram of Two-Stage Inverter.

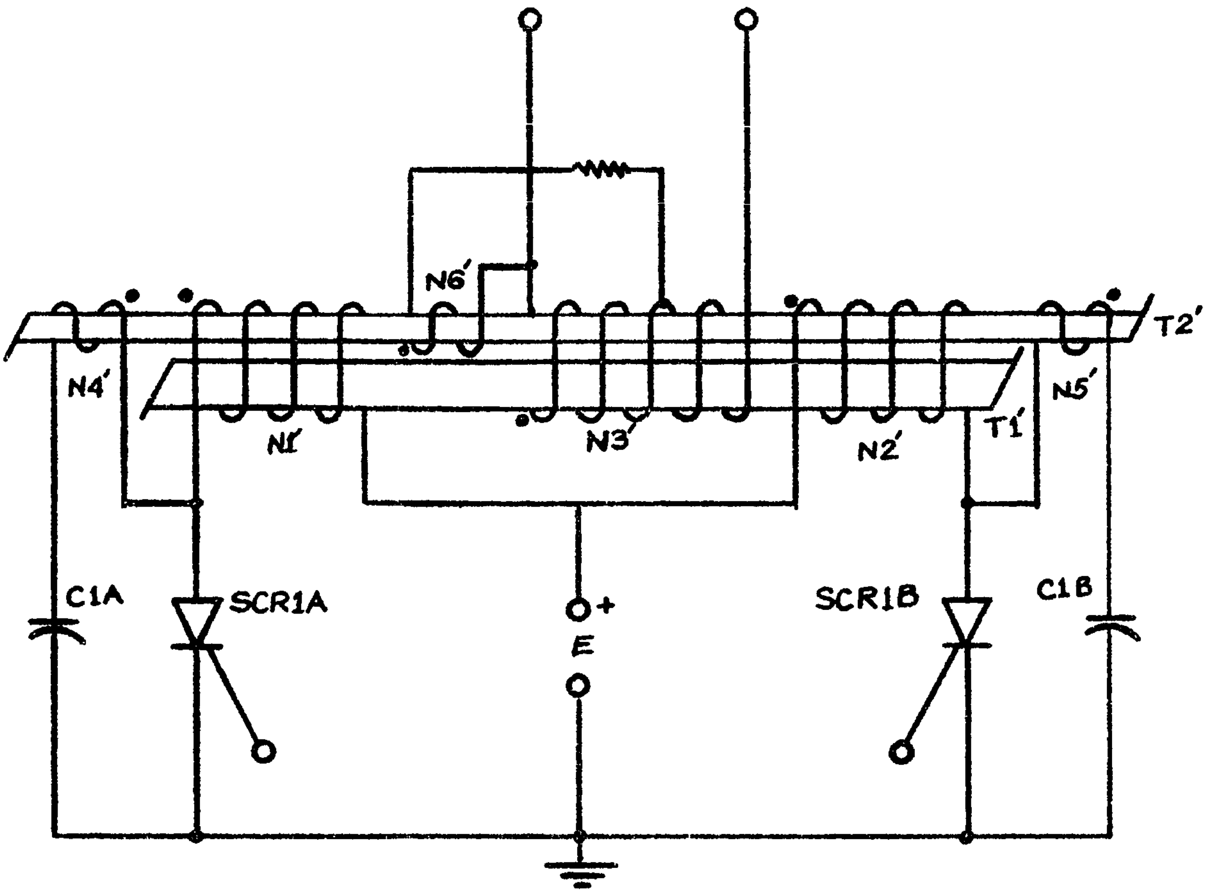


Fig. 8 Inverter Stage #1.

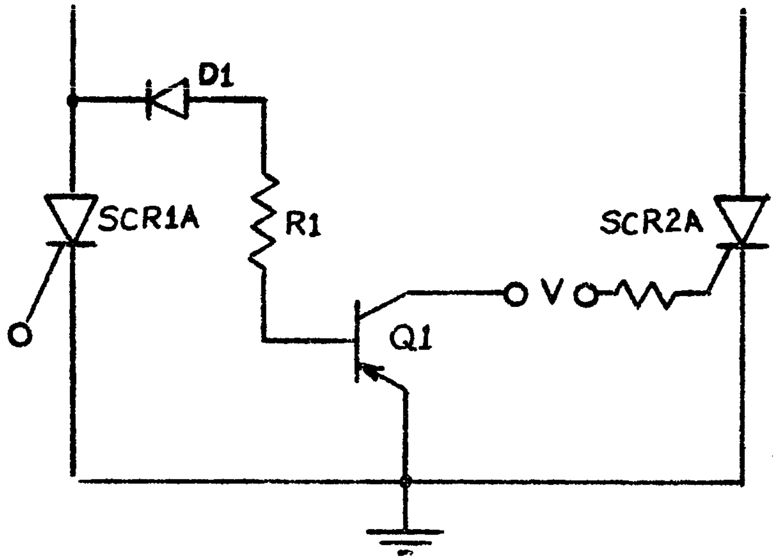
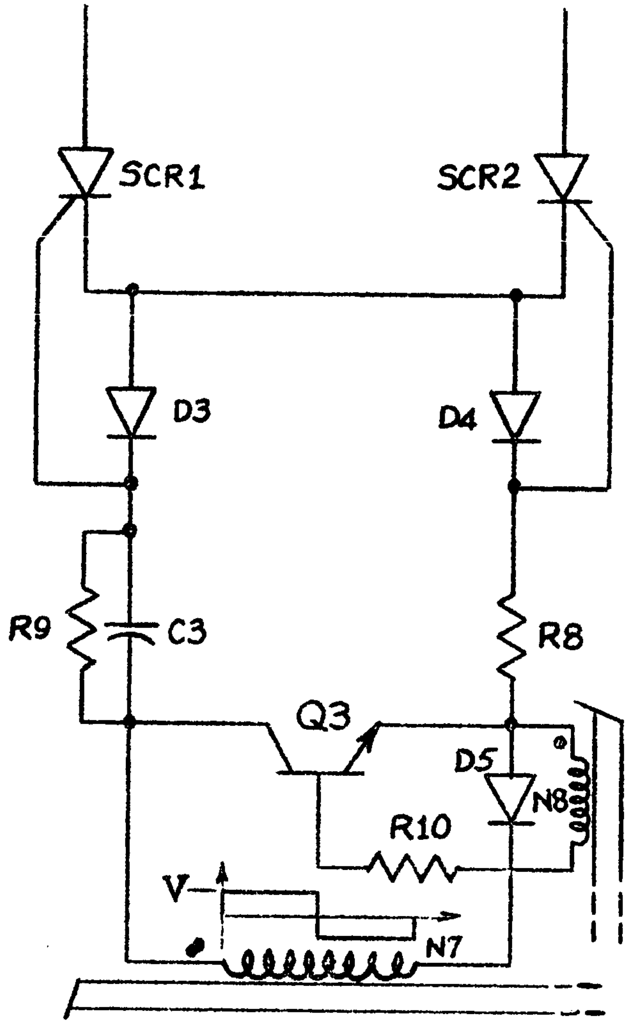


Fig. 9 Triggering One SCR From Another.



OUTPUT WINDINGS FROM
ROYER CIRCUIT

Fig. 10 First-Pulse Directing Circuit.

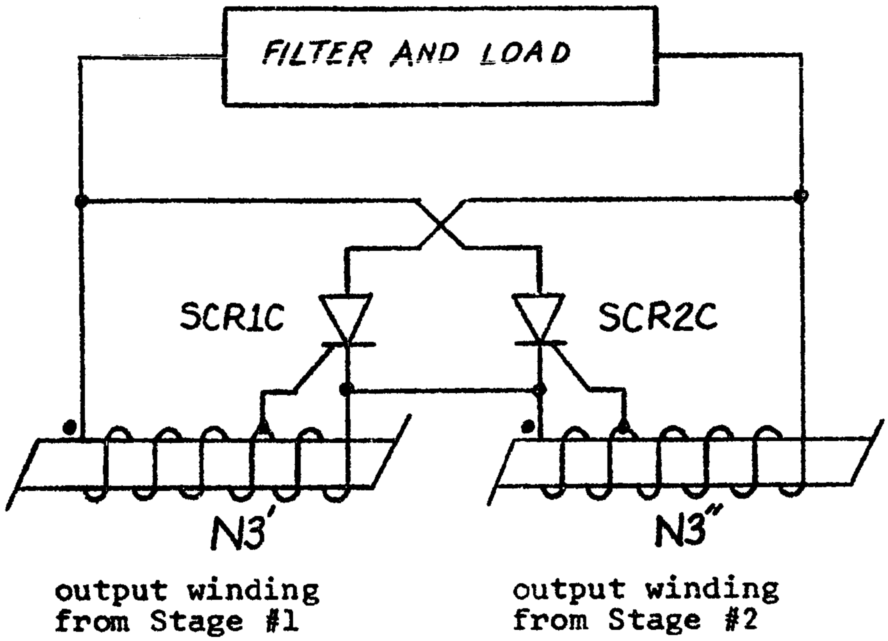


Fig. 11 Output Circuit

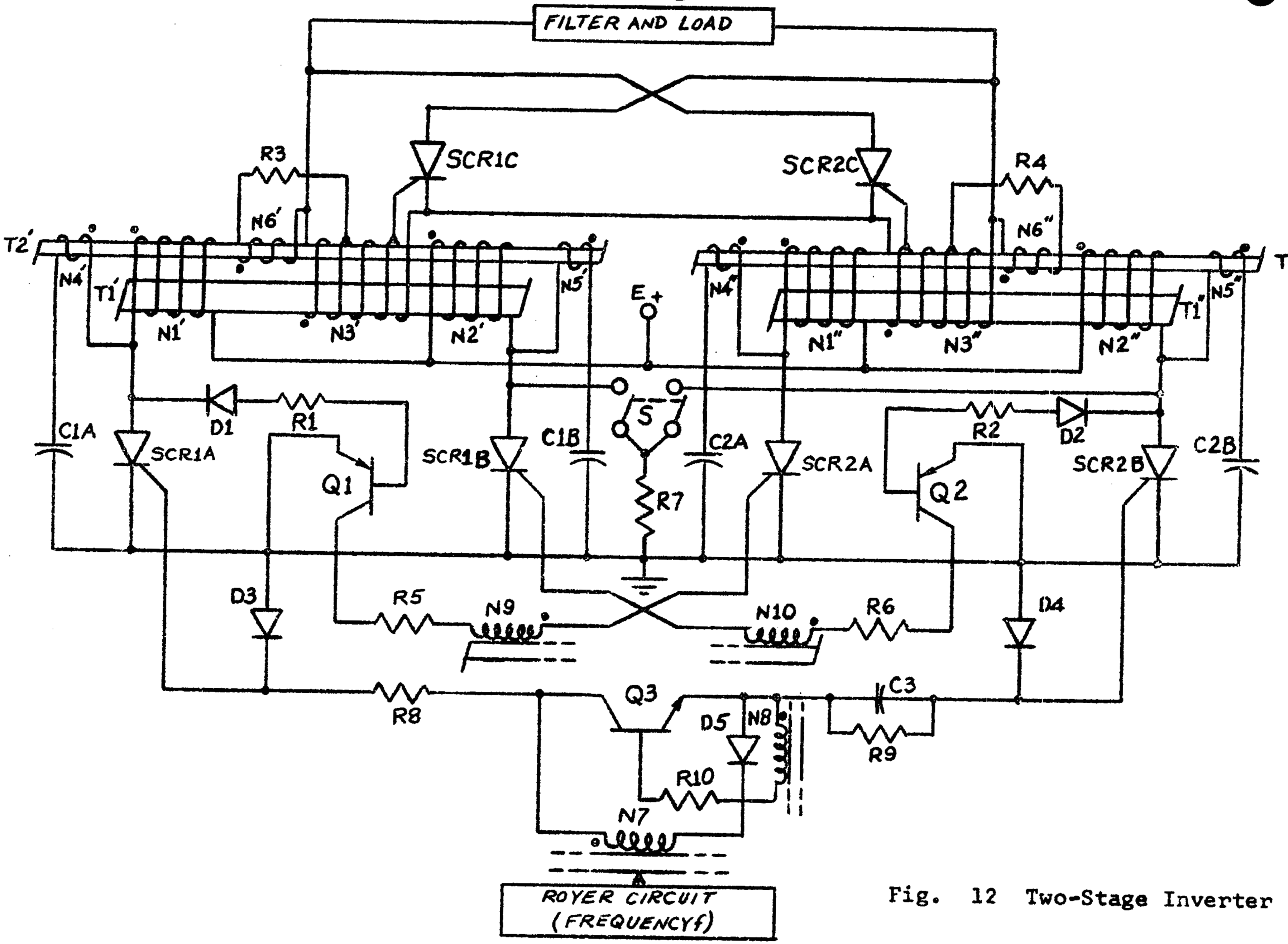


Fig. 12 Two-Stage Inverter